[0082] Figure 65 is a high level logical flowchart of an exemplary method of performing a global bus kill operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0083] Figure66 is a high level logical flowchart of an exemplary method of performing a local bus DCBZ operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0084] Figure67 is a high level logical flowchart of an exemplary method of performing a global bus DCBZ operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0085] Figure 68 is a high level logical flowchart of an exemplary method of performing a local bus castout operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0086] Figure 69 is a high level logical flowchart of an exemplary method of performing a global bus castout operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0087] Figure 70 is a high level logical flowchart of an exemplary method of performing a local bus write operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention;

[0088] Figure 71 is a high level logical flowchart of an exemplary method of performing a global bus write operation in a data processing system implementing Tn and Ten coherency states in accordance with the present invention; and

[0089] Figure 72 is a high level logical flowchart of an exemplary method of performing a global bus partial write operation in a data processing system implementing Tn and Ten coherency states in